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TO: Assistant Commissioner for Patents
Box Patent Applications
Washington D.C. 20231

Attorney Docket No.089048/167
(must include alphanumeric codes if no inventors named)

UTILITY PATENT APPLICATION TRANSMITTAL
(new nonprovisional applications under 37 CFR 1.53(b))

Transmitted herewith for filing is the patent application of:

INVENTOR(S): Joseph CHEN, Hung-Wen CHEN, and Michael CHEN

TITLE: INTEGRATED CIRCUIT DEVICE HAVING A CORE CONTROLLER, A BUS BRIDGE, A GRAPHICAL CONTROLLER AND A UNIFIED MEMORY CONTROL UNIT BUILT THEREIN FOR USE IN A COMPUTER SYSTEM

In connection with this application, the following are enclosed:

APPLICATION ELEMENTS:

XX Specification - 21 TOTAL PAGES

(preferred arrangement:)

-Descriptive Title of the Invention
-Cross Reference to Related Applications
-Statement Regard Fed sponsored R&D
-Reference to Microfiche Appendix
-Background of the Invention
-Brief Summary of the Invention
-Brief Description of the Drawings (if filed)
-Detailed Description
-Claim(s)
-Abstract of the Disclosure

XX Drawings - Total Sheets 7

XX Declaration and Power of Attorney - Total Sheets 5

XX Newly executed (original or copy)

___ Copy from a prior application (37 CFR 1.63(d))

(relates to continuation/divisional boxes completed) - NOTE: Box below

___ DELETION OF INVENTOR(S) - Signed statement attached deleting inventor(s) named in the prior application, see 37 CFR 1.63(d)(2) and 1.33(b).

_____ Incorporation By Reference (useable if copy of prior application Declaration being submitted)

The entire disclosure of the prior application, from which a COPY of the oath or declaration is supplied as noted above, is considered as being part of the disclosure of the accompanying application and is hereby incorporated by reference therein.

_____ Microfiche Computer Program (Appendix)

_____ Nucleotide and/or Amino Acid Sequence Submission (if applicable, all necessary)

____ Computer Readable Copy
____ Paper Copy (identical to computer copy)
____ Statement verifying identify of above copies

ACCOMPANYING APPLICATION PARTS

XX Assignment Papers (cover sheet & document(s))
____ 37 CFR 3.73(b) Statement (when there is an assignee)
____ English Translation Document (if applicable)

____ Information Disclosure Statement(IDS) with PTO-1449. _ Copies of IDS Citations
____ Preliminary Amendment
_XX_ Return Receipt Postcard (MPEP 503)
_XX_ Small Entity Statement(s)
___ Statement file in prior application, status still proper and desired.
____ Certified Copy of Priority Document(s) with Claim of Priority (if foreign priority is claimed).
____ OTHER: Check for $420.00

If a **CONTINUING APPLICATION**, **check appropriate box and supply the requisite information:**
__ Continuation __ Divisional __ Continuation-in-part (CIP) of prior application Serial No. __.

__ Amend the specification by inserting before the first line the following sentence: --This application is a __ continuation, __ divisional or __ continuation-in-part of application Serial No. __, filed __.--

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FEE CALCULATIONS: (Small entity fees indicated in parentheses.)

(1) For	(2) Number Filed	(3) Number Extra	(4) Rate	(5) Basic Fee $760 ($380)
Total Claims	7 - 20 =	0	x $18 (x $9)	0.00
Independent Claims	1 - 3 =	0	x $78 (x $39)	0.00
Multiple Dependent Claims			$260 ($130)	0.00
Assignment Recording Fee per property			$40	40.00
			TOTAL FEE:	$420.00

METHOD OF PAYMENT:
A check in the amount of the above TOTAL FEE is attached. If payment is enclosed, this amount is believed to be correct; however, the Commissioner is hereby authorized to charge any deficiency or credit any overpayment to Deposit Account No. 19-0741.

Respectfully submitted,

S. A. Bent

Stephen A. Bent
Reg. No. 29,768

Date: November 25, 1998
Docket No.: 089048/167

INTEGRATED CIRCUIT DEVICE HAVING A CORE CONTROLLER, A BUS BRIDGE, A GRAPHICAL CONTROLLER AND A UNIFIED MEMORY CONTROL UNIT BUILT THEREIN FOR USE IN A COMPUTER SYSTEM

BACKGROUND OF THE INVENTION

1. Field of the Invention

The invention relates to an integrated circuit device for use in a computer system, more particularly to an integrated circuit device that has a core controller, a bus bridge, a graphical controller and a unified memory control unit built therein.

2. Description of the Related Art

Referring to Figure 1, a conventional personal computer system 1 is shown to comprise a central processing unit (CPU) 10, a host bus 11 connected to the CPU 10, a core logic 12 connected to the host bus 11, a memory bus 13 connected to the core logic 12, a system memory 14 connected to the memory bus 13, an input/output (I/O) bus 15 connected to the core logic 12, at least one peripheral device 16 connected to the I/O bus 15, an Advanced Graphical Port (AGP) bus 17 connected to the core logic 12, a stand-alone video graphic accelerator (VGA) card 18 connected to the AGP bus 17, and a monitor 19 connected to the VGA card 18. The VGA card 18 includes a VGA chip 181, a local frame buffer 182 formed from dynamic memory, and a flash memory 183 for VGA BIOS.

Referring to Figure 2, it has been proposed heretofore in another conventional personal computer system 2 to discard the stand-alone VGA card, and mount the VGA chip 281 and the local frame buffer 282 directly on the system board (not shown) to reduce costs and simplify manufacture of the system board.

Referring to Figure 3, it has also been proposed heretofore in still another conventional personal computer system 3 to employ a unified memory architecture (UMA) in order to result in more cost savings by reducing the system board space and the components on the system board (not shown). As shown, the personal computer system 3 comprises a CPU 30, a host bus 31 connected to the CPU 30, a core logic 32 connected to the host bus 31, an I/O bus 35 connected to the core logic 32, at least one peripheral device 36 connected to the I/O bus 35, an AGP bus 37 connected to the core logic 32, a VGA chip 38 connected to the AGP bus 37, a shared system memory 34, and a wired-or memory bus 33 interconnecting the core logic 32, the VGA chip 38 and the shared system memory 34. Since the VGA chip 38 shares the system memory 34 with the core logic 32, the need to provide a dedicated local frame buffer for the VGA chip 38 is therefore obviated.

However, in order to enable the VGA chip 38 and the core logic 32 to share the system memory 34, some protocol must be introduced for the VGA chip 38 and the

core logic 32 to follow. There is thus a need to incorporate additional pins and interface signals into the VGA chip 38 and the core logic 32 for protocol communication. Referring again to Figure 3, the VGA chip 38 issues the MREQ# signal to inform the core logic 32 of its need to use the memory bus 33 for data transmission. After internal arbitration by the core logic 32, the core logic 32 releases the memory bus control to the VGA chip 38, and indicates the released state to the VGA chip 38 via the MGNT# signal. At this time, the memory access cycle of the VGA chip 38 can proceed as long as the MGNT# signal is driven to an active state by the core logic 32. The memory access cycle of the VGA chip 38 is terminated when the MGNT# signal becomes inactive, except in cases where the VGA chip 38 issues a high priority signal (not shown) to the core logic 32.

Furthermore, since there is a switching penalty whenever the memory bus control is switched from the core logic 32 to the VGA chip 38, and vice versa, the wired-or architecture of the memory bus 33 will downgrade the system performance. Figure 4 shows detailed pin constructions of the memory control signals which are driven by the core logic 32 and the VGA chip 38 onto the memory bus 33 for data transmission. Figure 5 shows the switching overhead that is incurred whenever the memory bus 33 is switched between the core

logic 32 and the VGA chip 38. As illustrated, the time period T1 between activation of the MREQ# signal and activation of the MGNT# signal depends on whether or not the memory bus is idle and on the internal arbitration algorithm of the core logic 32. The length of the time period T2, i.e. the length of the MGNT# signal, depends on the VGA data transmission length and on the presence of a memory request from other master devices with a higher priority than the VGA chip 38. In time period T3, if there is a memory request from another master device with a higher priority, the core logic 32 will cease to assert the MGNT# signal to inform the VGA chip 38 to stop its data transmission by deactivating the MREQ# signal. Otherwise, the core logic 32 will only cease to assert the MGNT# signal after the VGA chip 38 has finished its data transmission and has inactivated the MREQ# signal.

Because the memory bus 33 has the wired-or architecture, when one of the core logic 32 and the VGA chip 38 assumes control of the memory bus 33, it becomes responsible for driving all control signals to the system memory 34 to ensure proper functioning of the latter. Whenever the control of the memory bus 33 is switched from one master to another, the original master of the memory bus 33 should drive all the control signals of the memory bus 33 to a high voltage level for at least one clock cycle, and subsequently float

the memory bus 33 by deactivating the output (o/p) enable pins of the corresponding memory bus signals (see Figure 4) to avoid bus contention. In this manner, at least four clock signals are wasted due to bus switching when the control of the memory bus 33 is switched from one master to another. Moreover, in order to meet timing requirements of the system memory 34, such as RAS# pre-charge time, both the core logic 32 and the VGA chip 38 must finish the RAS# pre-charge time before they switch the memory bus 33 and after they get control of the memory bus 33 in order to avoid compatibility issues in the event that the core logic 32 and the VGA chip 38 are made by different chip vendors.

It is also noted that the conventional personal computer system 3 involves overhead in translating data from one bus protocol to another bus protocol, i.e. the generation of data in the form of the destination bus protocol. Synchronization penalty is further incurred if the clock domain of the source bus is different from that of the destination bus.

Translating the host data destined for the VGA chip 38 in the conventional personal computer system 3 normally comprises three phases: the initiate phase, the translated phase, and the response phase. The initiate phase starts from the cycle request from a current host bus owner to the generation of an

intermediate request. The translated phase starts from the intermediate request to the completion of the cycle on the destination bus. The response phase starts from the completion of the cycle by a response agent on the destination bus to the completion of the cycle on the originating bus. In most cases, the initiate phase on the originating bus and the response phase on the destination bus perform at different clock domains. In the conventional personal computer system 3 of Figure 3, the initiate phase is performed on the 100MHZ X86-like host bus 31, while the response phase is performed on the 66MHz AGP bus 37.

Therefore, in the event of an incoming transaction to the AGP bus 37, synchronization must be performed before entering the translated phase owing to communication between the two different clock domains. Figure 6 illustrates a synchronizer 39 for performing the aforesaid synchronizing function. The synchronizer 39 is separated into an input stage 391 and an output stage 392. The input signal at the input stage 391 is sampled using an input clock. The output signal of the input stage 391 serves as an input to the output stage 392, and is sampled using an output clock. The penalty of the synchronization process depends on the skew between the input and output clocks. As shown in Figure 7, if the rising edge of the output clock is near the rising edge of the input clock, less penalty is paid

for the synchronization process, as indicated by the output signal (A) in Figure 7. Otherwise, if the rising edge of the output clock is far from the rising edge of the input clock, more penalty is paid for the synchronization process, as indicated by the output signal (B) in Figure 7.

Upon entering the translated phase for an AGP bus transaction after the synchronization process, the VGA chip 38 accepts the transaction and drives the response. Before entering the response phase, the communicating signal must be synchronized owing to communication between the two different clock domains. This synchronization process is the same as that between the initiate and translated phases, the main difference residing in the switching of the definitions of the input and output clocks.

SUMMARY OF THE INVENTION

Therefore, the object of the present invention is to provide an integrated circuit device for use in a personal computer system so as to overcome the aforesaid drawbacks that are commonly associated with the conventional personal computer systems.

More particularly, the main object of the present invention is to provide an integrated circuit device that has a core controller, a bus bridge, a graphical controller and a unified memory control unit built therein, whereby not only is the system cost reduced,

but the need for a wired-or logic connection between the memory control unit and the system memory can be eliminated as well so as to eliminate the penalty paid in switching from the system memory controller to the display memory controller, and vice versa, for optimum graphical performance.

Another object of the present invention is to provide an integrated circuit device of the aforementioned type which includes separate internal buses that interconnect the core controller, the bus bridge, the graphical controller, and the unified memory control unit and that are operable concurrently, whereby the synchronization overhead that is commonly encountered when translating data from one bus protocol to another bus protocol can be eliminated to enhance the performance of a personal computer system.

According to this invention, an integrated circuit device is adapted for use in a computer system that includes a processing unit, a host bus connected to the processing unit, an input/output bus, a peripheral device connected to the input/output bus, a monitor, and a system memory. The integrated circuit device comprises a core controller adapted to be connected to the host bus, a bus bridge connected to the core controller and adapted to be connected to the input/output bus, a graphical controller connected to the core controller and the bus bridge and adapted to

be connected to the monitor, and a unified memory control unit connected to the core controller and the graphical controller and adapted to be connected to the system memory. The core controller, the bus bridge, the graphical controller and the unified memory control unit are built into a single integrated circuit package.

In the preferred embodiment, the unified memory control unit includes a graphical-memory address/data path connected to the graphical controller, a system-memory address/data path connected to the core controller, a centralized memory arbiter connected to the core controller and the graphical controller so as to detect a respective memory request signal therefrom, and a unified memory controller adapted to be connected to the system memory and connected to the graphical-memory and system-memory address/data paths, the unified memory controller being further connected to and controlled by the memory arbiter so as to be adapted to allocate access of the system memory to one of the graphical controller and the core controller via a corresponding one of the address/data paths in accordance with status of the memory request signals received by the memory arbiter.

Preferably, three separate and concurrently operable internal buses connect the graphical controller and a respective one of the core controller,

the bus bridge and the unified memory control unit. The internal buses run at the same clock domain as the host bus.

BRIEF DESCRIPTION OF THE DRAWINGS

Other features and advantages of the present invention will become apparent in the following detailed description of the preferred embodiment with reference to the accompanying drawings, of which:

Figure 1 is a schematic circuit block diagram of a conventional personal computer system that incorporates a stand-alone VGA card;

Figure 2 is a schematic circuit block diagram of another conventional personal computer system that has a VGA chip and a local frame buffer mounted directly on a system board;

Figure 3 is a schematic circuit block diagram of still another conventional personal computer system that has a core logic and a VGA chip connected to a shared system memory via a wired-or memory bus;

Figure 4 shows detailed pin constructions of the memory control signals which are driven by the core logic and the VGA chip of the conventional personal computer system of Figure 3 onto the wired-or memory bus for data transmission;

Figure 5 shows the switching overhead that is incurred whenever the wired-or memory bus is switched between the core logic and the VGA chip in the

conventional personal computer system of Figure 3;

Figure 6 illustrates a synchronizer that is employed in the conventional personal computer system of Figure 3;

Figure 7 illustrates the penalty that is introduced by the synchronizer of Figure 6; and

Figure 8 is a schematic circuit block diagram of the preferred embodiment of an integrated circuit device for use in a personal computer system in accordance with the present invention.

DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring to Figure 8, the preferred embodiment of an integrated circuit device 5 according to the present invention is shown to be adapted for use in a personal computer system that comprises a CPU 40, a host bus 41 connected to the CPU 40, an input/output (I/O) bus 42, peripheral devices connected to the I/O bus 42, a monitor 44, and a system memory 45. The peripheral devices include a video capture card 431 and a south bridge 432 connected to a USB port device 433, a hard disk drive (IDE) 434, and a read-only memory (ROM) 435 for system BIOS and VGA BIOS. The integrated circuit device 5 includes a core controller 50, a bus bridge 51, a graphical controller 52 and a unified memory control unit 53 that are built into a single integrated circuit package.

The core controller 50 is adapted to be connected to the host bus 41, and functions as a host bus interface, a host command queue, and a read/post-write first-in first-out (FIFO) memory.

The bus bridge 51 is adapted to be connected to the I/O bus 42, and is interfaced to the core controller 50 via a first internal bus 510, thereby permitting transmission of data from the host bus 41 to the I/O bus 42, and vice versa.

The graphical controller 52 is adapted to be connected to the monitor 44, and functions as a graphical command queue, a graphical engine, a read-ahead/post-write FIFO memory, a cathode ray tube (CRT) FIFO memory, a texture cache and a CRT controller. A second internal bus 520 interfaces the graphical controller 52 and the core controller 50, and is responsible for transferring configuration data, I/O data, command data, and frame buffer data from the core controller 50 to the graphical controller 52, and vice versa. The destination of the configuration data, the I/O data, and the command data are normally to and from a FIFO memory in the graphical controller 52. The destination of the frame buffer data is the part of the system memory 45 that is allocated as the display memory. However, the frame buffer data is normally temporarily stored in the write FIFO memory or read FIFO memory of the graphical controller 52 before being sent to the

system memory 45 or forwarded to the second internal bus 520.

In the preferred embodiment, a third internal bus 522 interfaces the graphical controller 52 and the bus bridge 51. Video data from the I/O bus 42 is written into the system memory 45 via the bus bridge 51, the third internal bus 522 and the graphical controller 52. Normally, the video data is written temporarily in the FIFO memory of the graphical controller 52 before being sent to the system memory 45.

The unified memory control unit 53 includes a graphical-memory address/data path 530 interfaced to the graphical controller 52 via a fourth internal bus 524, a system-memory address/data path 531 interfaced to the core controller 50 via a fifth internal bus 500, a centralized memory arbiter 532 connected to the core controller 50 and the graphical controller 52 so as to detect a respective memory request signal (REQ) therefrom, and a unified memory controller 533 adapted to be connected to the system memory 45. The unified memory controller 533 is further connected to the graphical-memory and system-memory address/data paths 530, 531, and to the memory arbiter 532. According to the status of the memory request signals (REQ) received by the memory arbiter 532, the memory controller 533 is controlled by the memory arbiter 532 so as to be adapted to allocate access of the system memory 45 to

one of the graphical controller 52 and the core controller 50 via a corresponding one of the address/data paths 530, 531.

For instance, when the graphical controller 52 processes commands that are queued therein, memory access requests are generated to the memory arbiter 532 to retrieve data from the system memory 45 or to write data into the system memory 45. Data transfer, inclusive of periodic screen refresh data, computed graphical data, and frame buffer data, between the graphical controller 52 and the unified memory control unit 53 is accomplished via the fourth internal bus 524. The fourth internal bus 524 is also used to transfer texture data stored in the system memory 45 to the texture cache of the graphical controller 52.

Since the internal buses 510, 520, 522, 524, 500 are separate, data transactions on these internal buses can be performed simultaneously for multiple data transaction. For instance, command data can be performed in the second internal bus 520 simultaneous with the transfer of texture data in the fourth internal bus 524. This is in contrast with the conventional personal computer system 3 shown in Figure 3, where the command data and the texture data cannot be performed simultaneously through the single AGP bus 37. Moreover, command data can be performed in the second internal bus 520 simultaneous with the transfer of video data

in the third internal bus 522. In the conventional personal computer system 3 of Figure 3, video data from the I/O bus 35 can only be transferred to the system memory 34 through the AGP bus 37, thereby impeding concurrent operation of command data and video data.

Furthermore, almost no overhead is paid in translating data from one bus protocol to another bus protocol in the integrated circuit device 5 of the present invention since the graphical controller 52 is connected to each source or destination bus via the internal buses 520, 522, 524, thereby obviating the need to translate the data that originates on the source bus to the bus protocol in the destination bus. In the instance of data from the host bus 41 to the graphical controller 52, only the intermediate replica of the data is generated at the internal bus 520 to minimize the overhead. Note that the clocks paid for generating the intermediate request from the host bus 41 to the internal bus 520, and vice versa, are the only overhead incurred. However, these clocks are generated naturally due to interfacing of the host bus 41 and the graphical controller 52. By running the internal buses 510, 520, 522, 524, 500 at the same clock domain as the source bus, such as the host bus 41, the need for a synchronization process in the initiate phase and the response phase of the graphical controller 52 can be completely eliminated. Upon comparing with the

conventional personal computer system 3 of Figure 3, the total number of clocks spent in the initiate and response phase by the integrated circuit device 5 is the same, but the number of clocks spent in the translated phase is tremendously reduced in the integrated circuit device 5 of this invention because the synchronization process and the data translation process have been eliminated.

In other words, the integrated circuit device 5 of the present invention increases the data throughput from the source bus to the destination bus because time is spent in forwarding data between the two buses instead of translating the data between the two buses.

It has thus been shown that the integrated circuit device 5 of this invention offers the benefit of lower system cost because the number of pins that are in use is dramatically reduced. Moreover, since the need for a wired-or logic connection between the integrated circuit device 5 and the system memory 45 has been eliminated with the provision of the unified memory control unit 53, the penalty paid in switching from a system memory controller to a display memory controller, and vice versa, is eliminated to improve the overall system performance. In addition, the synchronization overhead that is commonly encountered when translating data from one bus protocol to another bus protocol can be eliminated to further enhance the performance of the

personal computer system that incorporates the integrated circuit device 5 of the present invention. The objects of the present invention are thus achieved.

While the present invention has been described in connection with what is considered the most practical and preferred embodiment, it is understood that this invention is not limited to the disclosed embodiment but is intended to cover various arrangements included within the spirit and scope of the broadest interpretation so as to encompass all such modifications and equivalent arrangements.

WHAT IS CLAIMED IS:

1. An integrated circuit device for use in a computer system that includes a processing unit, a host bus connected to the processing unit, an input/output bus, a peripheral device connected to the input/output bus, a monitor, and a system memory, said integrated circuit device comprising:

a core controller adapted to be connected to the host bus;

a bus bridge connected to said core controller and adapted to be connected to the input/output bus;

a graphical controller connected to said core controller and said bus bridge and adapted to be connected to the monitor; and

a unified memory control unit including: a graphical-memory address/data path connected to said graphical controller; a system-memory address/data path connected to said core controller; a centralized memory arbiter connected to said core controller and said graphical controller so as to detect a respective memory request signal therefrom; and a unified memory controller adapted to be connected to the system memory and connected to said graphical-memory and system-memory address/data paths, said unified memory controller being further connected to and controlled by said memory arbiter so as to be adapted to allocate access of the system memory to one of said graphical

controller and said core controller via a corresponding one of said address/data paths in accordance with status of the memory request signals received by said memory arbiter.

2. The integrated circuit device as claimed in Claim 1, wherein said core controller, said bus bridge, said graphical controller and said unified memory control unit are built into a single integrated circuit package.

3. The integrated circuit device as claimed in Claim 1, further comprising three separate and concurrently operable internal buses that connect said graphical controller and a respective one of said core controller, said bus bridge and said unified memory control unit.

4. The integrated circuit device as claimed in Claim 3, wherein said internal buses run at the same clock domain as the host bus.

5. The integrated circuit device as claimed in Claim 1, further comprising:

a first internal bus that interfaces said core controller and said bus bridge;

a second internal bus that interfaces said graphical controller and said core controller;

a third internal bus that interfaces said graphical controller and said bus bridge;

a fourth internal bus that interfaces said graphical controller and said unified memory control unit; and

a fifth internal bus that interfaces said core controller and said unified memory control unit.

6. The integrated circuit device as claimed in Claim 5, wherein said first, second, third, fourth and fifth internal buses are separate from each other and are operable concurrently.

7. The integrated circuit device as claimed in Claim 5, wherein said first, second, third, fourth and fifth internal buses run at the same clock domain as the host bus.

ABSTRACT OF THE DISCLOSURE

An integrated circuit device is adapted for use in a computer system that includes a processing unit, a host bus connected to the processing unit, an input/output bus, a peripheral device connected to the input/output bus, a monitor, and a system memory. The integrated circuit device includes a core controller adapted to be connected to the host bus, a bus bridge connected to the core controller and adapted to be connected to the input/output bus, a graphical controller connected to the core controller and the bus bridge and adapted to be connected to the monitor, and a unified memory control unit connected to the core controller and the graphical controller and adapted to be connected to the system memory.

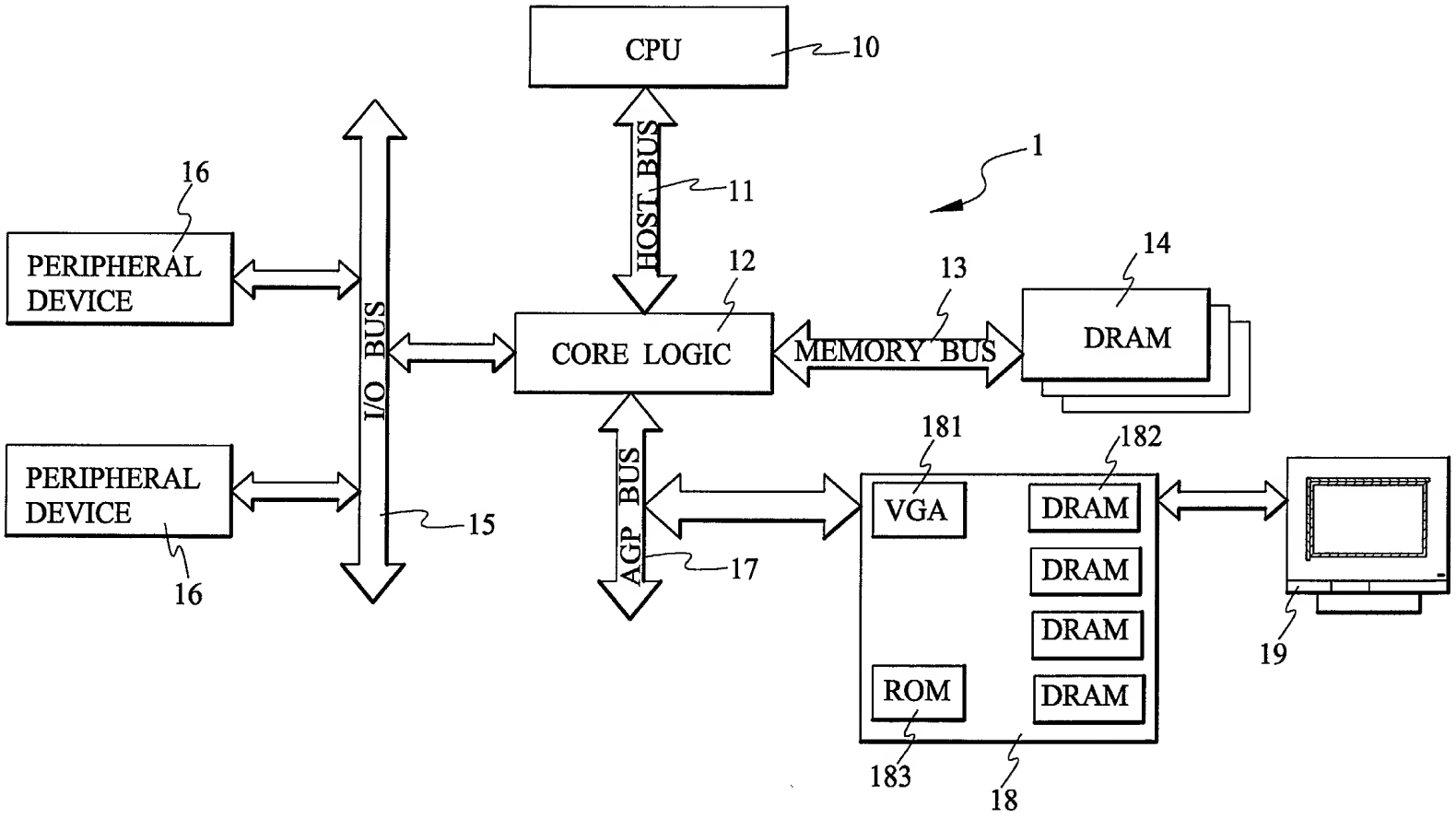

FIG. 1 PRIOR ART

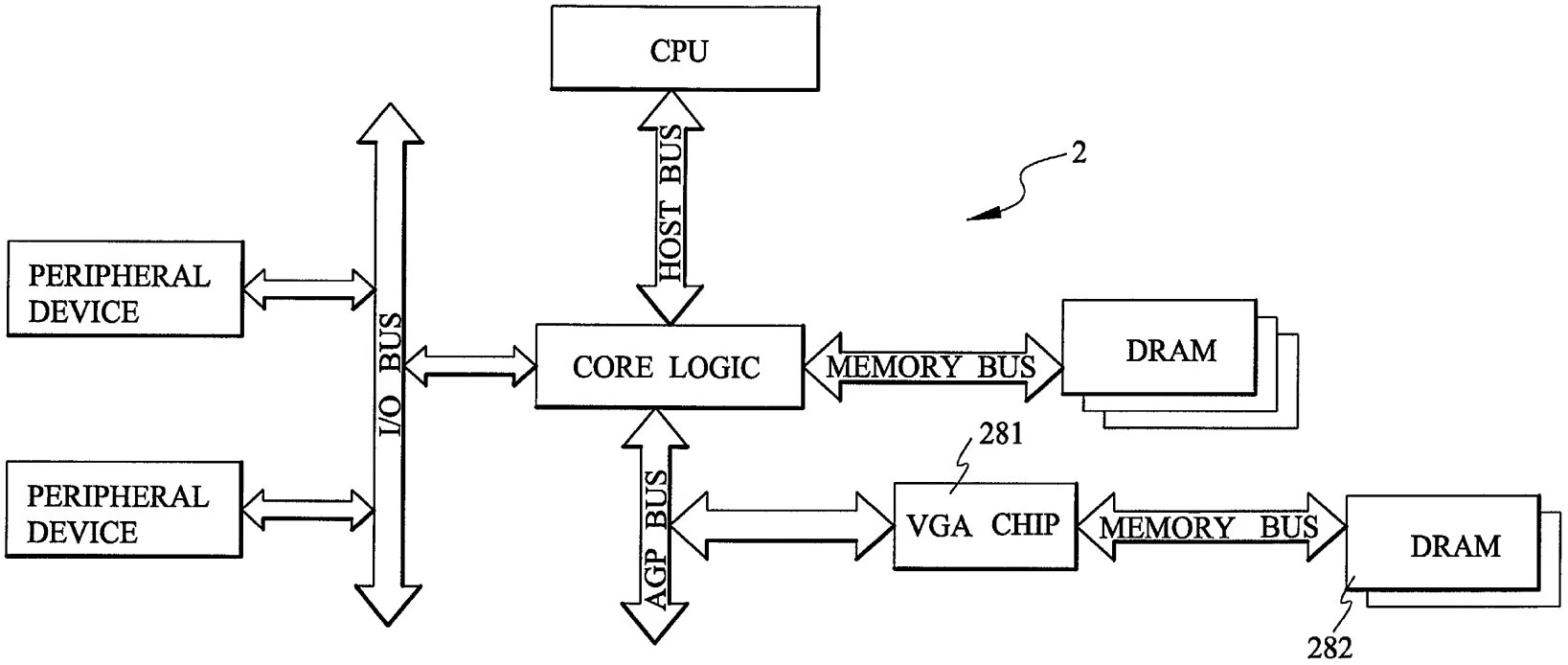

FIG.2 PRIOR ART

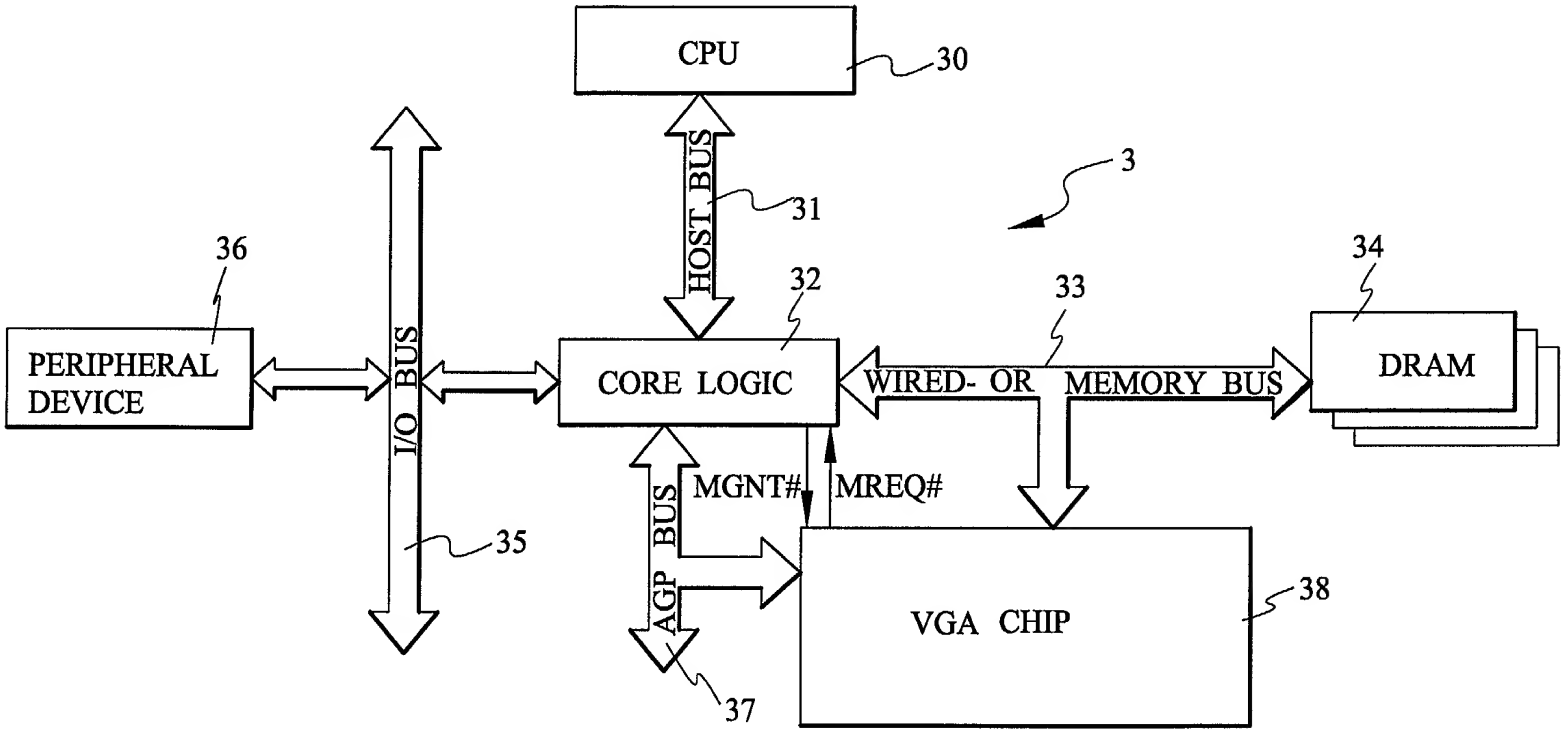

FIG.3 PRIOR ART

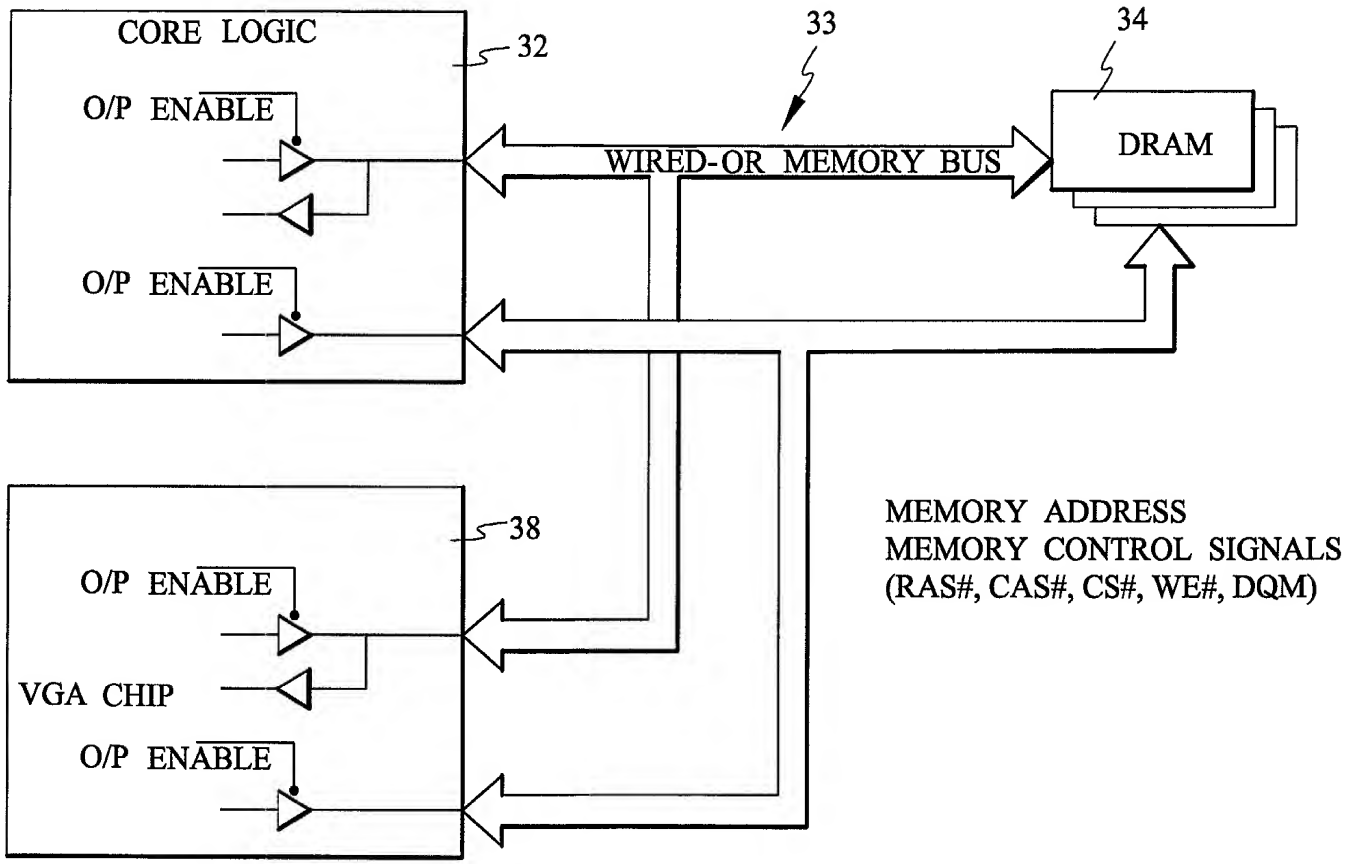

FIG.4 PRIOR ART

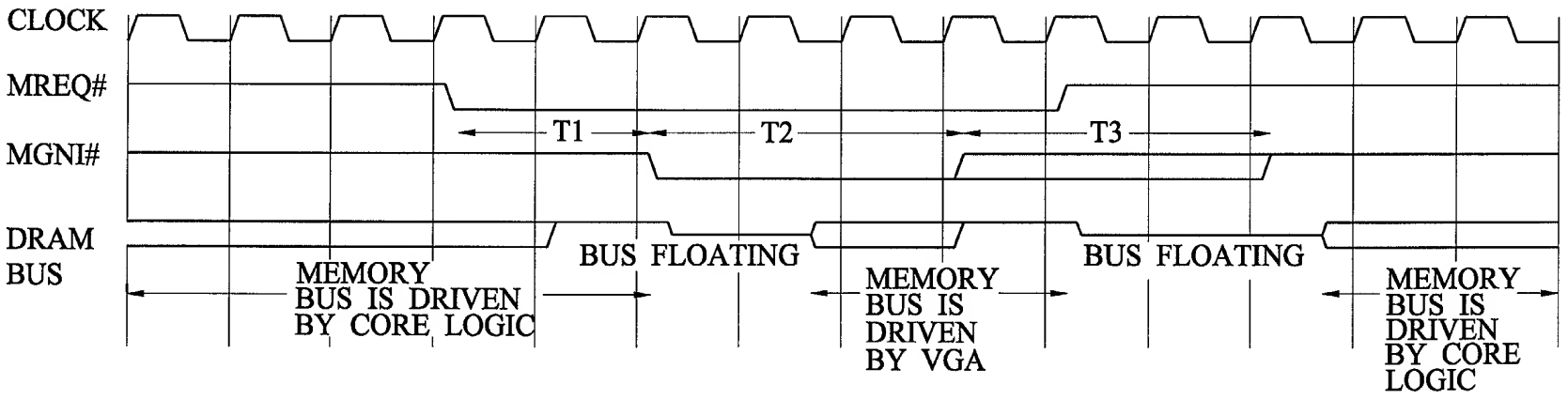

FIG.5 PRIOR ART

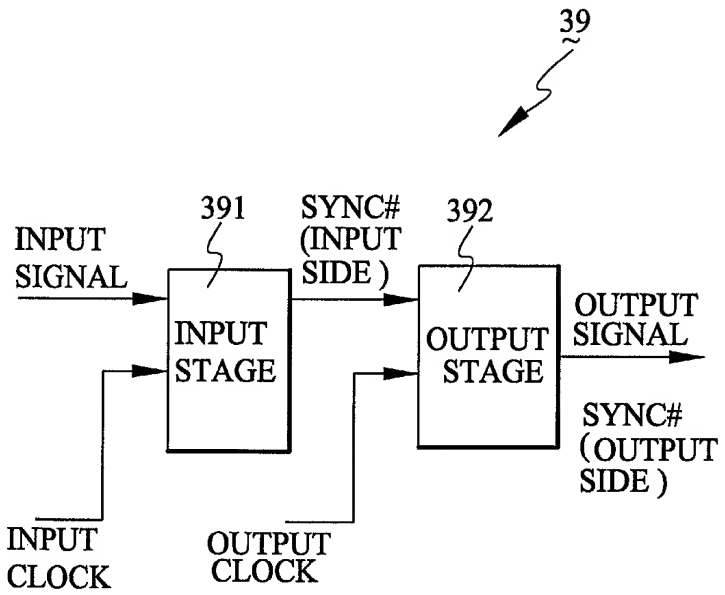

FIG.6 PRIOR ART

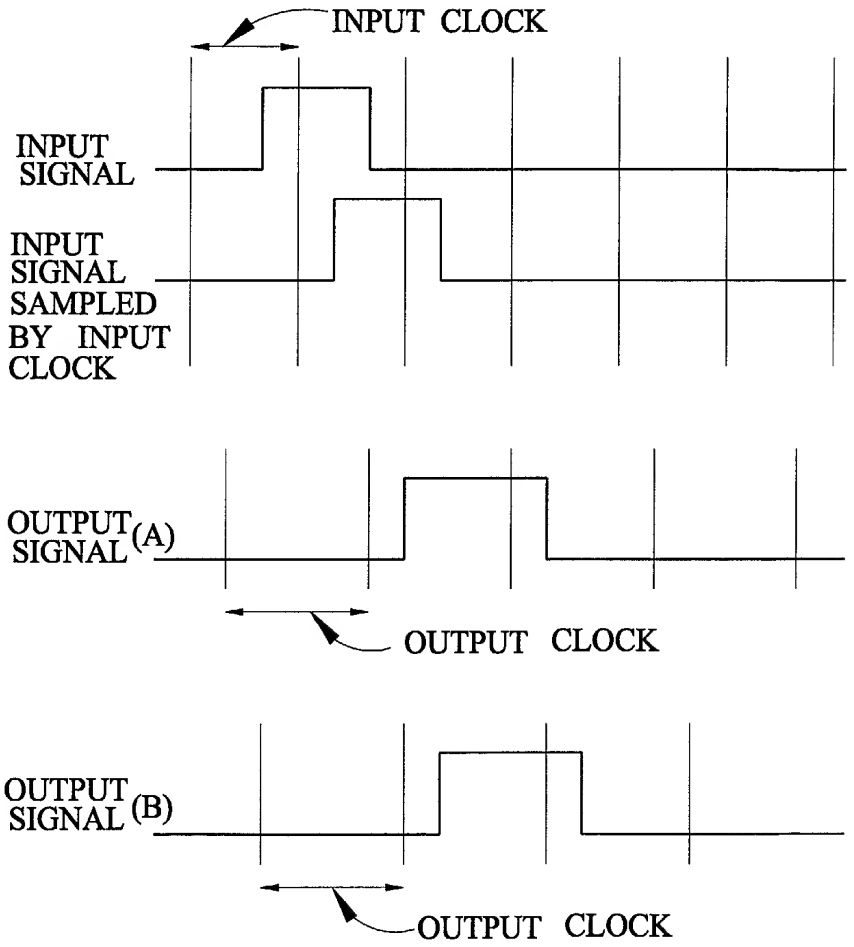

FIG.7 PRIOR ART

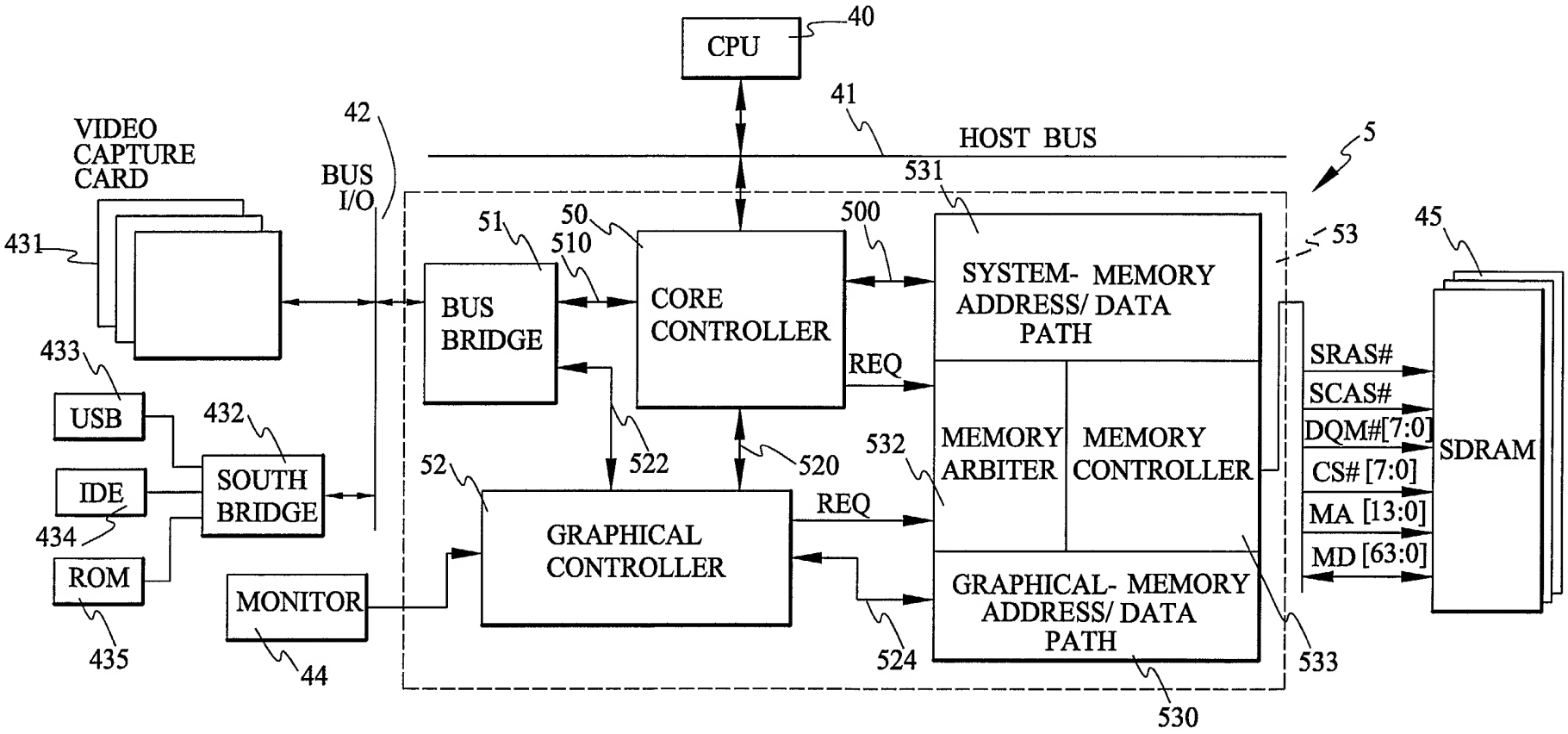

FIG.8

Declaration and Power of Attorney For Patent Application
專利申請聲明及委托書
Chinese Language Declaration
中文聲明

作爲下述聲明者，我在此宣告：

我的住址、郵局地址和國籍均列在我名下：

我相信我是首創的、第一個和唯一的聲明者(如只列出一人姓名)或是首創的、首位共同發明者(如列出數人姓名)。我提出作爲專利申請權利要求的題目如下：

_____

_____

_____

如不在下面小方格中打叉則須將說明書附此：

☐ 以美國申請號碼或PCT國際申請號碼_____
立案于_____
修正于(如適用)_____

我在此聲明我已閱讀並理解上述說明書的內容,包括上述任何修正案所修正的權利要求。

按照聯邦法規第三十七節第一．五六條，我有責任提供支持專利權的實質性資料。

As a below-named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled

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the specification of which is attached hereto unless the following box is checked:

☐ was filed on _____
as United States Application Number or PCT International Application Number
_____ and was amended on
_____ (if applicable).

I hereby state that I have reviewed and understand the contents of the above-identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37 Code of Federal Regulations, § 1.56..

Chinese Language Declaration

我申請享受按照美國法規三十五節第一百一十九條列出的以下任何外國專利申請書或發明者証書的外國優先權，並確認下列具有優先權申請前立案日期的、任何外國專利申請書或發明者証書。

I hereby claim foreign priority under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor's certificate listed below and have also identified below any foreign application for patent or inventor's certificate having a filing date before that of the application on which priority is claimed.

(號碼) (Number)	(國名) (Country)	(申請日/月/年) (Day/Month/Year Filed)	是否要求優先權 是 Yes	否 No
NONE			☐	☐
			☐	☐
			☐	☐

我申請享受按照美國法規第三十五節一百二十條列出的以下任何美國申請書的利益，如果此申請書中提出的每項權利要求的題目未按美國法規第三十五節第一百二十條第一段的要求在以前的美國申請書中披露，則我有責任按照聯邦法規第三十七節第一．五六(甲)條提供支持專利權的實質性資料，這一法規條文生效于以前申請的立案日期之後，但在美國或PCT國際申請立案日期之前。

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulations, § 1.56 which became available between the filing date of the prior application and the national or PCT International filing date of this application:

(申請順序號碼) (Application Serial No.)	(申請日期) (Filing Date)	(狀況) (已獲專利權、申請中、取消)	(Status) (patented, pending, abandoned)

我在此聲明根據我所知而作的所有聲明都眞實無誤，所有有關資料和信息的聲明也眞實無誤;我還知道，按照美國法規第十八節第一千零一項，任何蓄意偽造的聲明都將受到罰款或監禁，或同時受到兩種懲罰。這類蓄意偽造的聲明將危及此申請書或任何已頒發專利的效力。

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Chinese Language Declaration

委托書：
以列名發明者的身份，我在此指定下列律師和/或代理人執行此申請並從事與專利商標公署有關的所有業務(列出姓名和注冊號碼)：

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorney(s) and/or agents(s) to prosecute this application and transact all business in the Patent and Trademark Office connected therewith. *(list name and registration number)*

Please see attachment

回信請寄：

Send Correspondence to:
FOLEY & LARDNER
Suite 500
3000 K Street, N. W,
Washington, D. C. 20007-5109
U.S.A.

直撥電話(姓名及電話號碼)

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第一個或唯一的發明者全名	Full name of sole or first inventor Joseph CHEN
發明者簽字 日期	Inventor's signature Date Nov. 6, 1998
地址	Residence Hsin-Chu City, Taiwan
國籍	Citizenship Taiwan
郵局地址	Post Office Address 4F-2, No. 268, Wu-Ling Rd., Hsin-Chu City,
	Taiwan
第二個共同發明者全名(如有)	Full name of second joint inventor, if any Hung-Wen CHEN
第二個發明者簽字 日期	Second Inventor's signature Date Hung-Wen Chen Nov. 6, 1998
地址	Residence Hsin-Chu City, Taiwan
國籍	Citizenship Taiwan
郵局地址	Post Office Address 4F, No. 110, Lane 89, Sec. 1, Kuang-Fu
	Rd., Hsin-Chu City, Taiwan

(第三個和其他共同發明者需提供同樣資料和簽字。) (Supply similar information and signature for third and subsequent joint inventors.)

Chinese Language Declaration

	Full name of third joint inventor, if any Michael CHEN
日期	Third Inventor's signature Date Michael T.H. Chen NOv. 6, 1998
地址	Residence Hsin-Chu City, Taiwan
國籍	Citizenship Taiwan
郵局地址	Post Office Address 4F, NO. 22, Lane 38, Pei-Ying St.,
	Hsin-Chu City, Taiwan

	Full name of fourth joint inventor, if any
日期	Fourth Inventor's signature Date
地址	Residence
國籍	Citizenship
郵局地址	Post Office Address

	Full name of fifth joint inventor, if any
日期	Fifth Inventor's signature Date
地址	Residence
國籍	Citizenship
郵局地址	Post Office Address

	Full name of sixth joint inventor, if any
日期	Sixth Inventor's signature Date
地址	Residence
國籍	Citizenship
郵局地址	Post Office Address

(第三個和其他共同發明者需提供同樣資料和簽字。) (Supply similar information and signature for third and subsequent joint inventors.)

Stephen A. Bent	Reg. No. 29,768
David A. Blumenthal	Reg. No. 26,257
John J. Feldhaus	Reg. No. 28,822
Donald D. Jeffery	Reg. No. 19,980
Peter G. Mack	Reg. No. 26,001
Sybil Meloy	Reg. No. 22,749
Brian J. McNamara	Reg. No. 32,789
Colin G. Sandercock	Reg. No. 31,298
Bernhard D. Saxe	Reg. No. 28,665
Richard L. Schwaab	Reg. No. 25,479
Arthur Schwartz	Reg. No. 22,115

Applicant or Patentee: 1. Joseph CHEN 2. Hung-Wen CHEN 3. Michael CHEN Attorney's
Serial or Patent No.: Docket No.:
Filed or Issued:
For: ~~INTEGRATED CIRCUIT DEVICE HAVING A CORE CONTROLLER, A BUS BRIDGE, A GRAPHICAL CONTROLLER AND A UNIFIED MEMORY CONTROL UNIT BUILT THEREIN FOR USE IN~~ A COMPUTER SYSTEM

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9 (f) and 1.27 (c)) — SMALL BUSINESS CONCERN

I hereby declare that I am

[X] the owner of the small business concern identified below:

[ ] an official of the small business concern empowered to act on behalf of the concern identified below:

NAME OF CONCERN SILICON INTEGRATED SYSTEMS CORP.

ADDRESS OF CONCERN No. 16, Creation Rd. I, Science-Based Insdustrial Park, Hsin-Chu City, Taiwan

I hereby declare that the above identified small business concern qualifies as a small business concern as defined in 13 CFR 121.3-18, and reproduced in 37 CFR 1.9 (d), for purposes of paying reduced fees under section 41(a) and (b) of Title 35, United States Code, in that the number of employees of the concern, including those of its affiliates, does not exceed 500 persons. For purposes of this statement, (1) the number of employees of the business concern is the average over the previous fiscal year of the concern of the persons employed on a full-time, part-time or temporary basis during each of the pay periods of the fiscal year, and (2) concerns are affiliates of each other when either, directly or indirectly, one concern controls or has the power to control the other, or a third party or parties controls or has the power to control both.

I hereby declare that rights under contract or law have been conveyed to and remain with the small business concern identified above with regard to the invention, entitled INTEGRATED CIRCUIT DEVICE HAVING A CORE CONTROLLER, A BUS BRIDGE, A GRAPHICAL CONTROLLER AND A UNIFIED MEMORY CONTROL UNIT BUILT THEREIN FOR USE IN A COMPUTER SYSTEM by inventor(s) 1. Joseph CHEN 2. Hung-Wen CHEN 3. Michael CHEN described in

[X] the specification filed herewith

[ ] application serial no. _____, filed _____.

[ ] patent no. _____, issued _____.

If the rights held by the above identified small business concern are not exclusive, each individual, concern or organization having rights to the invention is listed below* and no rights to the invention are held by any person, other than the inventor, who could not qualify as a small business concern under 37 CFR 1.9 (d) or by any concern which would not qualify as a small business concern under 37 CFR 1.9 (d) or a nonprofit organization under 37 CFR 1.9 (e).

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

NAME _____

ADDRESS _____

[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

NAME _____

ADDRESS _____

[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28 (b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

NAME OF PERSON SIGNING Sheau Ming Samuel Liu

TITLE OF PERSON OTHER THAN OWNER President

ADDRESS OF PERSON SIGNING No. 16, Creation Rd. I, Science-Based Insdustrial Park, Hsin-Chu City, Taiwan

SIGNATURE _____ DATE 4/6/98

Applicant or Patentee: 1. Joseph CHEN 2. Hung-Wen CHEN 3. Michael CHEN
Serial or Patent No.: _____ Attorney's Docket No.: _____
Filed or Issued: _____
For: INTEGRATED CIRCUIT DEVICE HAVING A CORE CONTROLLER, A BUS BRIDGE, A GRAPHICAL CONTROLLER AND A UNIFIED MEMORY CONTROL UNIT BUILT THEREIN FOR USE IN A COMPUTER SYSTEM

VERIFIED STATEMENT (DECLARATION) CLAIMING SMALL ENTITY STATUS (37 CFR 1.9 (f) and 1.27 (b)) — INDEPENDENT INVENTOR

As a below named inventor, I hereby declare that I qualify as an independent inventor as defined in 37 CFR 1.9 (c) for purposes of paying reduced fees under section 41 (a) and (b) of Title 35, United States Code, to the Patent and Trademark Office with regard to the invention entitled INTEGRATED CIRCUIT DEVICE HAVING A CORE CONTROLLER, A BUS BRIDGE, A GRAPHICAL CONTROLLER AND A UNIFIED MEMORY CONTROL UNIT BUILT THEREIN FOR USE IN A COMPUTER SYSTEM described in

[X] the specification filed herewith
[ ] application serial no. _____, filed _____
[ ] patent no. _____, issued _____

I have not assigned, granted, conveyed or licensed and am under no obligation under contract or law to assign, grant, convey or license, any rights in the invention to any person who could not be classified as an independent inventor under 37 CFR 1.9 (c) if that person had made the invention, or to any concern which would not qualify as a small business concern under 37 CFR 1.9 (d) or a nonprofit organization under 37 CFR 1.9 (e).

Each person, concern or organization to which I have assigned, granted, conveyed, or licensed or am under an obligation under contract or law to assign, grant, convey, or license any rights in the invention is listed below:

[ ] no such person, concern, or organization
[X] persons, concerns or organizations listed below*

*NOTE: Separate verified statements are required from each named person, concern or organization having rights to the invention averring to their status as small entities. (37 CFR 1.27)

FULL NAME SILICON INTEGRATED SYSTEMS CORP.
ADDRESS No. 16, Creation Rd. I, Science-Based Insdustrial Park, Hsin-Chu City, Taiwan
[ ] INDIVIDUAL [X] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

FULL NAME _____
ADDRESS _____
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

FULL NAME _____
ADDRESS _____
[ ] INDIVIDUAL [ ] SMALL BUSINESS CONCERN [ ] NONPROFIT ORGANIZATION

I acknowledge the duty to file, in this application or patent, notification of any change in status resulting in loss of entitlement to small entity status prior to paying, or at the time of paying, the earliest of the issue fee or any maintenance fee due after the date on which status as a small entity is no longer appropriate. (37 CFR 1.28 (b))

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under section 1001 of Title 18 of the United States Code, and that such willful false statements may jeopardize the validity of the application, any patent issuing thereon, or any patent to which this verified statement is directed.

Joseph CHEN	Hung-Wen CHEN	Michael CHEN
NAME OF INVENTOR	NAME OF INVENTOR	NAME OF INVENTOR
Joseph Chen	Hung-Wen Chen	Michael T.W. Chen
Signature of Inventor	Signature of Inventor	Signature of Inventor
Nov. 6, 1998	Nov. 6, 1998	Nov. 6, 1998
Date	Date	Date